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OVERLOADED CDMA CROSSBAR FOR NETWORK-ON-CHIP

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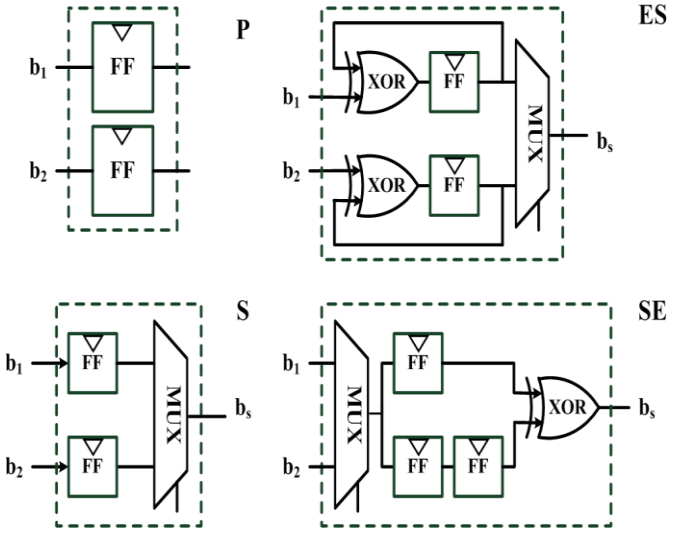
ABSTRACT: Here, in this project; embedded transition inversion (ETI) is proposed to reduce bit transitions in Serializing parallel buses. Implies power can be reduced further. This project proposes an embedded transition inversion (ETI) coding scheme that uses the phase difference between the clock and data in the transmitted serial data to tackle the problem of the extra indication bit. The technique is implemented in an optimized fashion using pipelining so that it can be used in practical systems with only a slight compromise in performance. This is achieved by calculating the decision as the data is being loaded on to the buffer and doing the encoding on the fly. This is one aspect which is lacking in most existing algorithms as they are not amenable to low delay implementation.

Keywords: ETI, TIC, Phase encoding, Tackle, B2I, Buffer, Serialized buffer, pipelining, Optimization.

INTRODUCTION: Low power design, in a system perspective, happens at all levels of the digital electronic system stack. It is being done from the lowermost device level design to the topmost software design. And there are the intermediate levels where a lot of effort is being expended to make systems run at low power, keeping the compromise in performance to be minimum. The increasing density of the integrated circuits as postulated by Moore's law makes it even more important to have low power systems since the power supply for such a densel integrated circuit may not keep track in size with the miniaturization of the electronic components. Hence research is being made at all levels of a system stack. A system can consist of multiple components. They can be broadly classified and a communication framework designed work.

BUS SCHEMES: There are four types of bus schemes, including parallel (P), serial (S), encoding followed by serial (ES), and serial followed by encoding (SE) as shown in Fig. Their average AFs are AFP,av, AFS,av, AFES,av, and AFSE,av , respectively. The bitstream in this paper refers to the transmitted data in each wire of the input parallel bus. The AF analysis results of serializing two bitstreams into a single output



EXSITING TECHNIQUE TO DESIGN BUS: (TIC) technique to reduce switching activity for random data and to detect errors. Their technique counts the transitions in the data word, and inverts the transition states if the number of transitions in a data word is more than half of the word length. The scheme sets the current bit in the serial stream to be the same as the previous encoded bit when there is a transition. Other wise, it is set to the inversion of the previous encoded bit. A transition indication

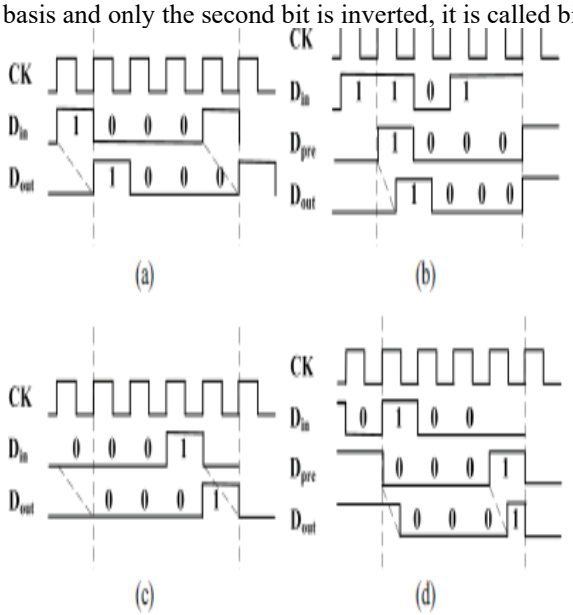
bit is added in every data word. This extra bit not only increases the number of transmitted bits, but also increases the transitions and latency. A serial link on-chip bus architecture is proposed to lower interconnect power [16]. Serialization reduces the number of wires and leads to a larger interconnect width and spacing. A large interconnect spacing reduces the coupling capacitance, while the wider interconnects reduce the resistivity. A significant improvement in the interconnect energy dissipation is achieved by applying different coding schemes and their proposed multiplexing techniques. However, the power reduction decreases when the degree of multiplexing increases. The embedded transition inversion (ETI) coding scheme to solve the issue of the extra indication bit [17]. This scheme eliminates the need of sending an extra bit by embedding the inversion information in the phase difference between the clock and the encoded data. When there is an inversion in the data word, a phase difference is generated between the clock and data. Otherwise, the data word remains unchanged and there is no phase difference between the clock and the data. This ETI coding scheme reduces transition by 31% compared with the SE scheme. The improvement of transition reduction is 19% compared with that of the TIC.

PROPOSED TECHNIQUE word exceeds the threshold Nth, the bits in the data word should be encoded. Otherwise, the data word remains the same. When an encoding is needed in a data word, this method checks every two-bit in the data word, as Fig. 3 shows. Every two bit in the serial stream is combined as a base to be encoded. In this case, the b11b21 is a base and the b31b41 is another base. The 2-bit in a base is denoted as b1b2 and the encoded output is denoted as be1be2. When the Nt in a data word is less than Nth, b1b2 remains unchanged. Otherwise, we perform the inversion coding and the phase coding. For the inversion coding, the bitstreams “01” and “10” are mapped to “00” and “11,” respectively. The bitstreams “00” and “11” are mapped to “01” and “10,” respectively. For the phase coding, we embed the inversion information in the phase difference between the clock and the encoded data.

$$b_{e1} = b_1$$

$$b_{e2} = \begin{cases} b_2, & \text{with } N_t < N_{\text{th}} \\ !b_2, & \text{with } N_t \geq N_{\text{th}}. \end{cases}$$

Since this operation is on a two-bit basis and only the second bit is inverted, it is called bit-two inversion (B2INV).



2) Phase Coding: The ETI coding uses the phase difference between the data and the clock to encode the indication information. The ETIpre has the same data word as the TIC, except that it removes the extra bit bex. Removing the bex leaves eight sets of data words that are exactly the same. For example, there are two “1000” data words after theETIpre coding.

Within every data word duration, the phase difference between the data and the clock distinguishes these twodata words, as Fig. 4 illustrates. Same Dout “1000” in If Din “1000” and “1101” without and with inversion. A half clock cycle difference between Dout and CK is shown in Fig. (b), indicating that Din has been encoded. The Dout and CK are aligned in Fig. (a), indicating that Din has not changed. Dout “0001” is the same in Fig. (c) and (d) from Din “0001” and “0100” without and with inversion. This approach is able to identify whether Dout has been encoded or not as long as there is a half cycle delay between the Dout and CK. Although the phase difference

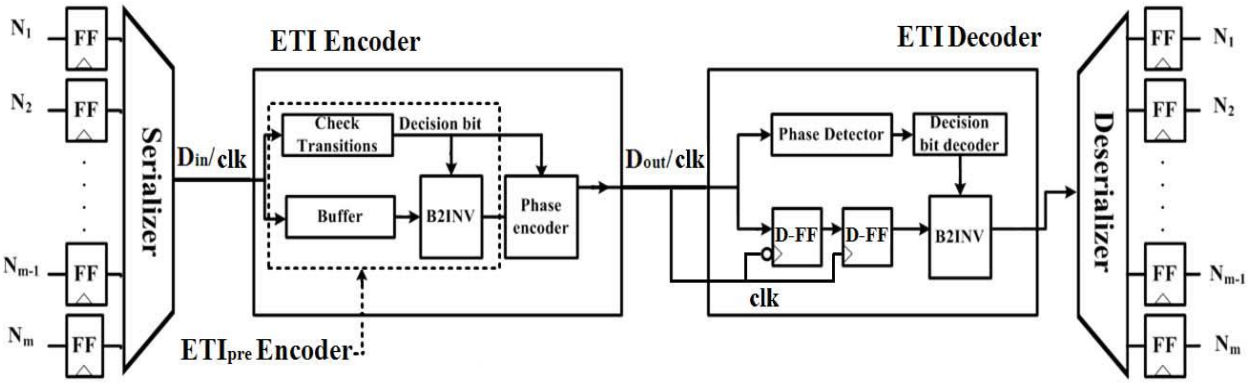
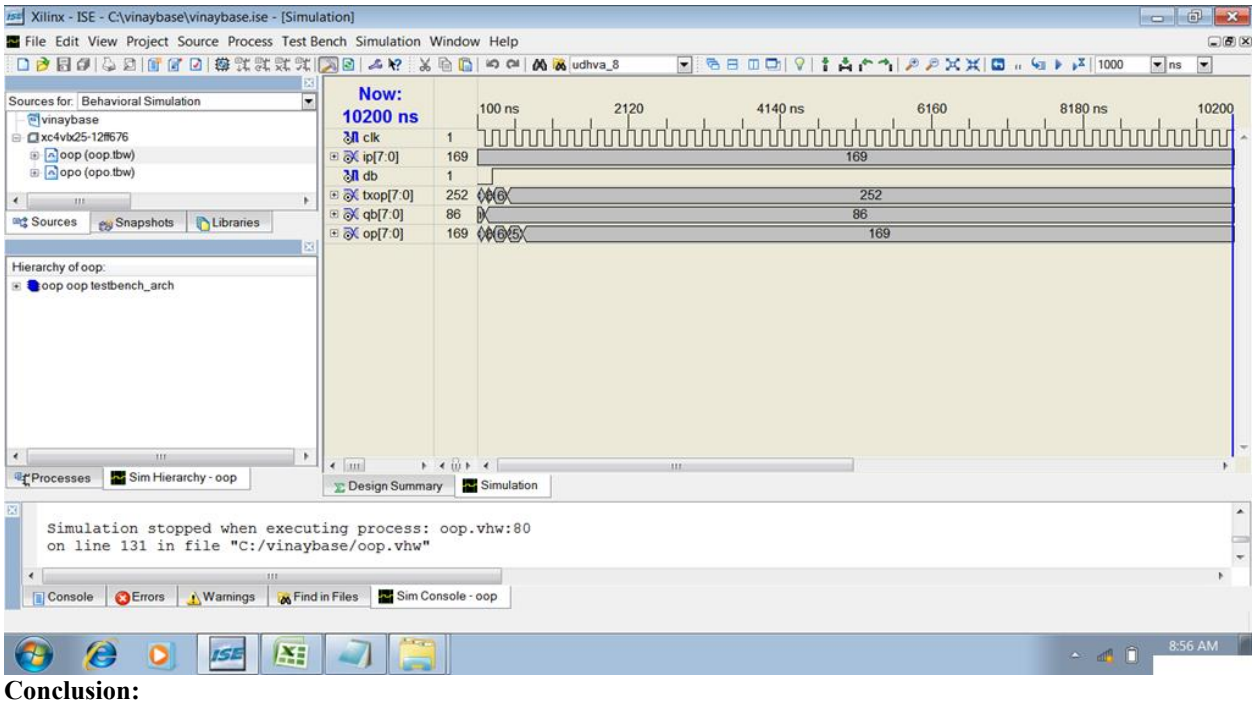


Fig: ETI Decoder

The ETI encoder generates the phase difference between the clock and the data word. Normally, a PD identifies an early or delayed phase. A variety of PDs could detect the phase difference. This paper adopts the commonly used Alexander PD [18]. The Alexander PD architecture is shown in Fig. (a), which uses three consecutive clock edges to generate four sampling signals (S0, S1, S2, and S3). The PD is controlled by the clock CK and input data Din. When the clock CK and input data Din are valid, the PD is activated to identify the phase relation between the clock and the data. The PD can determine whether a data transition exists from the condition that the clock leads or lags the data. The basic wave form is shown in Fig. (b) to judge the un-inverted, inverted, no transition, or the special data word. If the clock leads the data(early conditions), the signal S1 ⊕ S2 is high and the S2 ⊕ S3is low. Conversely, if the clock lags the data (late conditions), the signal S1 ⊕ S2 is low and S2 ⊕ S3 is high. Thus, S1 ⊕S2 and S2 ⊕ S3 could provide the clock and data relation are related.

S1 ⊕ S2	S2 ⊕ S3	Clock	Coding state
High	Low	Early	Has not been encoded
Low	Low	No transition	
Low	High	Late	Has been encoded
High	High	Special case	

RESULT:



Conclusion:

The ETI scheme is reduces the extra bit used in the TIC scheme and reduces the crosstalk, energy dissipation. ETI scheme uses the phase difference between the data and clock to indicate the bit inversion. In this project, the proposed ETI scheme is reduces

the area and power compare with the existing ETI scheme. This enhanced technique is more useful in multipurpose applications due to the reason that it has low latency, power consumption factors.

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